Reliability and Performance of 808nm Single Emitter Multi-Mode Laser Diodes

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ABSTRACT

Performance, lifetest data, as well as failure modes from two different device structures will be discussed in this paper, with emitting wavelengths from 780nm to 800nm. The first structure, designed for high temperature operation, has demonstrated good reliability on various packages with output power up to 10W from a 200 μ m emitting area. The device structure can be operated up to 60°C heatsink temperatures under CW conditions. Then a high efficiency structure is shown with further improvement on operation power and reliability, for room temperature operation. With ongoing lifetest at 12A and 50°C heatsink temperature, <1000 FIT has been achieved for 6.5W and 33°C operation, on both designs. MTT_{10%}F at 10W and 25°C operation is estimated to be more than 20,000 hours. Devices retain more than 20W rollover power under CW conditions, when re-tested after several thousand hours of accelerated lifetest. Paths for reliability improvement will also be discussed based on observed lifetest failure modes from these two structures.

Key words: Reliability, lifetime, life-test, high power lasers, high efficiency, high temperature, 808nm, 790nm, 780nm, semiconductor laser diodes

1. INTRODUCTION

High power diode lasers at near 800nm emission have been widely used for solid-state laser pumping, laser marking, materials processing and medical applications. The performance and reliability of diode lasers have been dramatically improved in the last decade [1-6]. For example, wall plug efficiency of ~70% has been reported through efforts such as Super High Efficiency Devices and Systems (SHEDS) program funded by DAPPA[1-2]. However, real system applications require more balanced performance attributes including power, efficiency at operation condition (not peak efficiency), high temperature performance and lifetime. Nowadays, increasing numbers of industry applications require the diodes to survive 2 years of around clock operation with less than 2% failure. In addition, devices at shorter wavelengths, near 780 and 790nm, are also sought for application such as Ho:Cr:Tm:YAG solid state laser pumping. Compared to devices in 9xxnm region [4-6], devices near 800nm have been much more difficult to achieve high power/brightness, wall plug efficiency, and reliability, due to intrinsic photon energy associated and material related issues.

This paper reports progress on single emitter broad area devices from 780nm to 820nm wavelength region. In particular, two different device configurations, high temperature (HT) structure and high efficiency (HE) structure have been investigated. Their operation power, efficiency, temperature performance, and lifetime will be presented. Tradeoffs among the performance attributes, as well as underlying mechanisms will be discussed. Lifetest failure modes for the different structures and paths for reliability improvement will also been addressed.

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2. EXPERIMENTS

All epitaxial structures were grown using low pressure MOCVD. Standard broad-area laser fabrication was used to process the wafers into chips with 200 μ m wide emitting areas and 3 mm long cavity lengths. Proprietary *n*XLT facet treatment technology, as well as PR/HR facet coating, was used for all devices. Then, chips were assembled onto various packages using hard solder on different types of conductive heatsinks. The packages include *n*Light's Pearl chiplets, CN mounts and conventional C-mounts. For both Pearl chiplets and CN mounts, chips were bonded onto electrically-insulating AlN submounts, which were further soldered on Cu carriers. While CN mounts, with bigger dimension, were designed for individual single emitter applications, Pearl chiplets were designed for fiber coupled modules that are based on multiple single emitters.

All devices went through initial test, burn in and post burn-in test. Various electrical and optical tests were performed after burn-in, including LIV (light-current-voltage), far field and near field under continuous wave (CW) conditions. Some of devices were also tested for Catastrophic Optical Mirror Damage (COMD) level under both CW and Quasi CW (QCW) conditions. QCW test were done with 3 μ sec pulse width and 1000 Hz frequency. All test equipments were calibrated following ISO standards. All voltage and resulted wall plug efficiency were measured directly from the devices, without subtracting package-associated resistances. Device's characteristic temperatures T₀ and T₁ were obtained through LIV test under pulse conditions at different temperatures.

Step stress lifetest for both temperature and current were carried out for initial reliability assessment. Then long-term accelerated lifetest was performed at 12A current and 50 °C heatsink temperature. Accurate junction temperatures and heatsink temperatures of the devices on lifetest racks were obtained by wavelength and thermocouple measurements on both test stations and lifetest racks. Techniques including microscope inspection on facets and epitaxial layer surface, electric-luminescence (EL) imaging, photoluminescence (PL) imaging were used for failure analysis.

3. RESULTS AND ANALYSIS

3.1 High temperature structure

For applications that require devices to operate at elevated temperatures, a structure was developed by tailoring epitaxial layer composition and thickness for strong carrier confinement. The structure providing medium fast axis far field, near 36 degree FWHM, was used to balance temperature performance and power/reliability. This structure was also optimized for devices to operate at various wavelengths ranging from 780nm to 820nm, by using optimal quantum well composition and thickness.

Figure 1a is the plot of LIV and typical spectrum curves at 25 °C heatsink temperature for devices bonded on Pearl chiplets. The figure contains data sets for devices operating at 780nm, 790nm and 808nm. As seen, all devices behaved similarly, reaching 10W near 9.6A. Their threshold currents are about 1.05A. Slope efficiencies are about 1.22W/A. The directly measured operation voltages are near 1.85V. Wavelength FWHM and FW1/e²W are about 1.7nm, 2.6nm respectively. Results from CN mount bonded devices were comparable as the thermal resistance of both packages are very similar. For devices bonded on C-mounts which have slightly higher thermal resistance, the device operation currents are also similar to those of chiplets or CN mounts. Figure 1b is the plot of LIV and typical spectrum curves at 60°C heatsink temperature, for the same devices as in Figure 1a. As seen, all devices can operate up to 15A, in spite of some degree of power roll over. The devices with longer wavelength have much less roll over than those with shorter wavelength. At 10A operating current, devices' wavelengths at 60°C heatsink temperature are about 8 nm longer than those at 25°C. Wavelength FWHM and FW1/e²M are about 1.7nm, 2.5nm respectively.



inserts. a): at 25°C heatsink temperature; b): at 60°C heatsink temperature

The different temperature behavior of devices at different wavelengths are also shown by the LIV curves tested under pulse condition at different temperatures, as well as associated T_0 and T_1 values. As seen in Figure 2, both T_0 and T_1 decrease with wavelength. This is due to the reduced bandgap offset between the quantum well and cladding layers for the shorter wavelength device. The T_0 and T_1 also have different values in different temperature ranges. In the temperature range from 15 °C to 60 °C, the T_0 and T_1 are 140-180 K and 500-730 K respectively. In the temperature range from 60 °C to 105 °C, the T_0 and T_1 are 100-140 K and 230-450 K respectively.



Figure 2: a). LIV curves under pulse condition at different temperatures for a HT device; b): T_0 and T_1 values of devices with various wavelengths for temperature ranging from 15 °C to 60 °C. c): T_0 and T_1 values of devices with various wavelengths for temperature ranging from 60 °C to 105 °C

Figure 3 summarizes wall-plug efficiencies. at both 25° C and 60° C heatsink temperatures, for the HT devices with different wavelengths. In spite of strong T₀ and T₁ dependency on operating wavelength, wall-plug efficiency at 7A are all near 56% at 25° C and 50% at 60°C heatsink temperature respectively, for wavelength range from 760nm to 820nm. The peak efficiencies are typically 1-3% higher than that at 7A.



Figure 3: Wall-plug efficiency for the HT devices with different wavelengths at 7A operating current, and at 25°C and 60°C heatsink temperatures.

To quickly assess lifetime performance, step stress lifetest was carried out at two different drive currents, 12A and 14A, by varying heatsink temperature from 60°C to 100°C and 50°C to 90°C, respectively. The corresponding junction temperatures are from 75°C to 115 °C at 12A and 70°C to 110 °C at 14A roughly. As shown in Figure 4, good devices can survive heatsink temperature up to 90°C at 12A drive current or 100 °C at 14A drive current. The temperature and current are limited by lifetest rack.



Figure 4: Step stress lifetest with HT devices, at heatsink temperature, from 50°C to 100°C, current set at: a). 12A; b). 14A.

Both CW and pulsed COMD test were also performed on the devices life-tested to various hours. After burn in, the devices show CW rollover levels about 20W at more than 20A. Pulsed COMD level is about 60W near 80A, as seen in Figure 5. The rollover/COMD levels were also sampled for devices aged for 2200 hours and 4700 hours in the 12A, 50 °C lifetest. As seen, the devices still show rollover without COMD even after 4700 hours of accelerated lifetest, which is equivalent to 39,300 hours operation at 10W and 25 °C or 211,500 hours at 6.5W and 33 °C, using an estimation method specified later.



Figure 5: a): CW COMD/rollover tests at 10 °C test station temperature, with various aging hours at 12A and 50 °C heatsink temperature; b): pulsed COMD test at 10 °C and under 3µm pulse width and 1000 Hz frequency pulse conditions

More than 500 devices have been life-tested at 12A and 50 °C heatsink temperature from 1500 hours to 10000 hours, with some of them terminated early due to lifetest rack capacity limitation. All failed devices show sudden failure, without slow degradation. Figure 6a and 6b present typical lifetest data for devices whose wavelengths at room temperatures are in 79x nm and 80x nm regions respectively. As seen, both groups show very low random failure prior to 6,000 hours of accelerated lifetime at 12A and 50 °C heatsink temperature, with only three out of forty devices failing randomly. Also, both groups show sudden wearout behavior after 6,000 hours of accelerated lifetime at 12A and 50 °C heatsink temperature. Using commercial reliability software, as well as Bellcore GR-468 standard, the lifetest data were analyzed. Figure 6c contains the probability plot of the lifetest data from both groups together. The data was also fitted through mix-Weibull model. Shape parameters obtained, β , are about 1 and 12 for two distinct regions, indicating two different failure modes, random failure and wear-out failure. The random failure follows an exponential distribution.





Figure 6: Accelerated lifetest for HT devices at 50 °C heatsink temperature and 12A: a): 20 devices with room temperature operating wavelength being at 79x nm; b): 20 devices with room temperature operating wavelength being near 808nm, 10 of them terminated at about 4000 hours; c): un-reliability plot of the lifetest data from both groups and associated mix-Weibull fits

Equivalent lifetime, under different conditions, as well as related failure rate was calculated using equation 1 as below

$$LT \propto LT_0 I^{-m} P^{-n} \exp\left(\frac{E_a}{k_B \cdot T_j}\right)$$
 (1)

Where, LT is the lifetime, LT_0 is a device based constant, I, P and T_j are current, power and junction temperature respectively. m and n are current and power acceleration factors. E_a is the activation energy and k_B is Boltzmann constant.

There are very limited data on the acceleration parameters from literature, especially for state-of-the-art devices near 800nm wavelength [3]. It takes many devices and a long time to obtain those parameters with a reasonable degree of confidence. In this paper, nominal parameters from literature, m=2, n=2, and $E_a=0.45$, were used. The calculated FIT with 90% confidence level, MTT_{10%}F with 90% confidence level, wear-out onset for the 40 devices presented above are 4900, 2.5 years, and 6.2 years respectively, for operating at 10W 25°C heatsink temperature. The FIT, MTT_{10%}F and wear-out onset time are 1000, 12 year, and 31 years respectively, for operating at 6.5W, 33 °C heatsink temperature.

Failure analysis on lifetest failures indicates that there are two failure modes. The COMD failure mode where failure originates from facet and bulk-defect initiated COD. In the random failure regime, both COD and COMD have been observed. In the wear-out regime, COMD is found to be the only failure mode. This is in contrast to those of devices in 9xx nm region [6], which usually do not have facet related wear-out for

state-of-the-art devices. This also validates that good facet passivation or similar techniques are essential for high reliability in 800nm devices.

3.2 High Efficiency Structure

Although the devices with the HT structure have yielded very good performance, higher wall plug efficiency and higher device operation power have been pursued. Super high efficiency SHEDS structures have been explored in the last several years [2]. Peak wall-plug efficiency has been demonstrated to be about 70% at lab conditions, with operation voltage being reduced dramatically. However the devices faced several challenges that affected their practical applications, including reliability, far field and high temperature performance. When high confinement factor is used to reduce threshold current, devices show large far field, small near field size in vertical direction and poor reliability. When small bandgap offset is used to reduce voltage the device's temperature performance is deteriorated. On the other side, super large optical cavity (SLOC) structure designs have been used to increase device's operation power and reliability by reducing internal loss, resulting in improved operation power and reliability. In this work, some of the approaches developed under SHEDS and the SLOC waveguide design, as well as HT design, are combined to produce a high efficiency (HE) structure for more balanced performance at room temperature.

Figure 7 contains LIV and wall-plug efficiency data of such a HE device, compared to those of a typical HT device. The operating wavelengths of both devices are near 808nm at room temperature. As seen, the slope efficiency of the HE device was around 1.27 W/A, compared to 1.22 W/A of HT device. The operating voltage of the HE device was near 1.81V, compared to 1.85V of a HT device. Threshold current of the HE device was around 1.15A, compared to 1.05A of a HT device. The peak wall plug efficiency of HE the device was about 63%, compared to 58% of the HT device. At 10W operation condition, the operation current and wall plug efficiency are 9A and 62% respectively. As shown in Figure 7c, HE devices show worse performance than HT devices at temperature above 60 °C. In the temperature range from 15 °C to 60 °C, HE device's T₀ and T₁ are 140 K and 730 K respectively, which are comparable to those of HT devices. In the temperature range from 60°C to 105 °C, however, HE device's T₀ and T₁ are 105 K and 370 K respectively, which are worse than those of HT devices near 808nm.





Figure 7: a). CW LIV curves of HE structure devices at 25°C heatsink temperature; b): LI and efficiency comparison of HE structure and HT structures; c). LIV curves under pulse condition at different temperatures for a device with HE structure

The far field (vertical axis) of the HE device, compared to the HT device, is shown in figure 8. As seen, the FWHM and $FW1/e^2W$ of the HE device is about 28° and 48° respectively, while those of the HT device are 36° and 62°, respectively. The reduced far field improves optical beam shaping and fiber coupling efficiencies.



Figure 8: Typical far field profiles (vertical axis) of HT and HE structures

The accelerated lifetest data of HE devices are shown in Figure 9. The devices have been running for about 7000 hours at 12A, and 50 °C heatsink temperature, without showing wear-out behavior. Under such conditions, device's output power was near 10.5W. Of the 20 devices on lifetest, two failed randomly. Using equation 1 and Bellcore GR-468 standard, the device failure rate is about 900 at 6.5W and 33 °C heatsink temperature. The calculated FIT with 90% confidence level, $MTT_{10\%}F$ at 90% confidence level, wear-out onset time are 4600, 2.6 years and > 7 years respectively, for 10W and 25 °C heatsink operation. The FIT, $MTT_{10\%}F$ and wear-out onset time are 900, 13 year and > 36 years respectively, for operation at 6.5W, 33 °C heatsink.

The failure analysis of the two failed devices showed they failed for bulk-defect initiated COD instead of COMD.



Figure 9: Accelerated lifetest for 20 HE devices performed at 50 °C and 12A driving current.

Thermal roll-over and COMD test were performed on the HE devices too. Figure 10a shows that the COMD level is 70W at 80A under pulse condition. This is about 15% higher than that of a HT device. Figure 10b shows the CW roll over test at 10 °C cold plate temperature at different stage of lifetime. Due to their higher efficiency HE device's roll-over power was close to 25W, which is about 20% higher than that of the HT device. The higher COMD/roll over power supports the longer wear out-onset time. The rollover/COMD level was also tested after the device was lifetested for about 3750 hours at 50 °C and 12A driving current. As seen in Figure 10b, the device still showed CW roll-over at about 23W without COMD even after 3750 hours of accelerated lifetest.



Figure 10: a): pulsed COMD test at °C and 3µm pulse width and 1000 Hz frequency; b): CW COMD/rollover test at 10 °C cold plate temperature, with various aging hours at 12A and 50 °C heatsink temperature

4. DISCUSSIONS

As presented above, both HT and HE devices have demonstrated very high power and high reliability. HT devices showed better high temperature performance. HE devices had smaller far field, higher power and higher efficiency at room temperature. These two structures allow us to choose optimal one for various applications. Due to design trade-offs, it is extremely challenging to have one structure with high temperature performance, efficiency, power and reliability all optimized at the same time.

While both HT and HE structures have demonstrated very low FIT values for random failure. HE structure has shown wear-out onset starts at a much later time, if there is any. No good accelerated lifetime models have been established for the state-of-the-art devices in 800nm region [3]. 7xx and 8xx nm devices show both random failure and wear-out failure, which can be modeled by exponential and lognormal or Weibull models respectively. The random failure has mainly been due to bulk defects in laser cavities. Although the majority of bulk defects can be screened out by burn in, some bulk defects took a much longer time to lead to device failures. Improved defect control in manufacturing processes, which are been pursued by institutions such as nLight, can reduce the bulk defect density and thus reduce device's failure rate FIT further. In addition, longer cavity length can reduce FIT score by reducing junction temperature and current density. The wear-out failure has been mainly shown as facet degradation. In the wavelength range between 780nm and 820nm, there exists a general trend that lifetime decreases with decreasing wavelength. It is believed that this is due to the intrinsic correlation between photon energy and non-radiative absorption. Reducing optical intensity on facet by techniques such as SLOC structure in vertical direction and flare structure in lateral direction, in addition to good facet passivation/coating technology, would increase device's power/brightness and wear-out lifetime. Near field profile and filamentation control can also increase device's power/brightness and wear-out lifetime.

5. CONCLUSIONS

HT design shows that the devices can operate up to 60°C heatsink temperature, while HE devices have shown higher wall-plug efficiency at room temperature. Both structures were shown to have very high COMD/rollover power even after stress testing. Their reliable operation can down to wavelengths as short as 780nm. Both HT and HE structures support 10W operation with $MTT_{10\%}F$ longer than two years. The failure rates at 6.5W, 33°C heatsink temperature were both near 1000 FIT. Random failure was shown to be dominated by bulk defects, while wear-out failure was shown to be facet dominated. Controlling bulk defects would improve FIT score further. Techniques that either reduce optical intensity on facet or improve the robustness of the facet would increase wear-out onset time.

ACKNOWLEDGEMENTS

This work was partially supported by US congressional funding.

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